

What is claimed is:

- Sub B1
1. A method for reducing random single bit data loss in a memory circuit comprising:  
providing a semiconductor layer having a surface;  
heating the layer in an atmosphere comprising a Hydrogen isotope; and  
fabricating a memory circuit using the semiconductor layer.
  2. The method of claim 1 and further comprising forming a film on the semiconductor layer that comprises the Hydrogen isotope.
  3. The method of claim 1 and further comprising fabricating a FLASH memory circuit using the semiconductor layer.
  4. The method of claim 1 and further comprising exposing the semiconductor layer to a temperature that oxidizes the semiconductor layer.
  5. The method of claim 1 and further comprising exposing the semiconductor layer to a temperature that anneals the semiconductor layer.
  6. The method of claim 1 and further comprising exposing the semiconductor, sequentially, to atmospheres comprising Hydrogen isotope and ammonia enriched in Hydrogen isotope at an elevated temperature.
  7. The method of claim 1 and further comprising fabricating a gate region within the memory circuit.
  8. The method of claim 7 and further comprising forming a film comprising Hydrogen isotope adjacent to the gate region of the memory circuit.
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- Sub A1
- Sub B3

9. The method of claim 7 and further comprising forming a film comprising Hydrogen isotope within the gate region of the memory circuit.

10. The method of claim 1 and further comprising passivating the semiconductor layer in an atmosphere comprising Hydrogen isotope.

11. The method of claim 1 and further comprising forming a field oxide in the semiconductor layer.

12. The method of claim 11 and further comprising annealing the field oxide layer in an atmosphere that comprises Hydrogen isotope or a Hydrogen isotope containing compound.

13. The method of claim 11 and further comprising annealing at a temperature that is at least about 800 degrees Centigrade.

14. The method of claim 11 and further comprising oxidizing the annealed field oxide layer in an atmosphere that comprises Hydrogen isotope.

15. An annealing atmosphere for annealing a semiconductor device with a FLASH memory comprising Hydrogen isotope and or a compound that comprises Hydrogen isotope.

17. The annealing atmosphere of claim 15 and further comprising water vapor.

18. The annealing atmosphere of claim 15 and further comprising an inert gas.

19. The annealing atmosphere of claim 15 and further comprising nitrogen or a compound comprising nitrogen.

20. A memory circuit, comprising:  
a main body comprising silicon;  
a memory cell disposed on and within the main body;  
a gate region proximal to the memory cell disposed on and within the main body; and  
a film disposed on or within the gate region, adjacent to the gate region or under the gate region, wherein the film comprises Hydrogen isotope.

21. The memory circuit of claim 20 wherein the memory cell is a FLASH memory.

22. The memory circuit of claim 20 wherein the film is a silicon dioxide film comprising Hydrogen isotope.

23. The memory circuit of claim 20 wherein the film is a silicon nitride film comprising Hydrogen isotope.

24. The memory circuit of claim 20 wherein the film comprises silicon dioxide and silicon nitride and Hydrogen isotope.

25. The memory circuit of claim 20 wherein the film comprises silicon oxynitride.

26. A method of forming a non-volatile electrically alterable semiconductor memory cell comprising:

providing a silicon substrate;  
fabricating a field oxide region and a channel region over or within the silicon substrate;  
growing an oxide over the channel region in an atmosphere enriched in Hydrogen isotope;

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fabricating at least one gate member; and  
passivating the memory cell in an atmosphere that comprises Hydrogen isotope.

27. The method of claim 26 and further including nitridizing the field oxide region by annealing in an atmosphere comprising Hydrogen isotope or a compound that comprises Hydrogen isotope.

28. The method of claim 26 and further comprising nitridizing at a temperature that is greater than or equal to about 800 degrees Centigrade.

29. The method of claim 26 and further including oxidizing the nitridized field layer in an atmosphere that comprises Hydrogen isotope.

30. The method of claim 26 and further comprising introducing the Hydrogen isotope by thermal oxidation.

31. The method of claim 26 and further comprising introducing the Hydrogen isotope by pyrolytic diffusion of Hydrogen isotope into the memory cell.

32. The method of claim 26 and further comprising introducing the Hydrogen isotope by RF sputter deposition.

33. A tunneling oxide component of a non-volatile, electrically alterable semiconductor memory cell, comprising Hydrogen isotope.

34. A thermal oxide component of a non-volatile, electrically alterable semiconductor memory cell, comprising Hydrogen isotope.

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35. A method for passivating a non-volatile, electrically alterable semiconductor memory cell, comprising:

providing a non-volatile, electrically alterable semiconductor memory cell;  
and  
exposing the memory cell to an atmosphere that comprises Hydrogen isotope.

36. The method of claim 35 and further including heating the atmosphere.

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37. A method for overlaying source and drain regions of a non-volatile, electrically alterable semiconductor memory cell with a thermal oxide layer, comprising:

providing a silicon substrate;  
defining source and drain regions; and  
growing the thermal oxide layer over the source and drain regions in an atmosphere that comprises Hydrogen isotope.

38. The method of claim 37 and further comprising heating the atmosphere that comprises Hydrogen isotope.

39. The method of claim 37 and further comprising defining the source and drain regions by targeted Hydrogen isotope implantation.